WHAT IS CLAIMED IS:

1. A DRAM-incorporated semiconductor device which has a DRAM section and a logic section being formed on one and the same substrate, wherein silicide layers are formed, at least, on all the surfaces of the source-drain regions and the gate surfaces of transistors in the DRAM section and the logic section.

2. The semiconductor device according to Claim 1, wherein said silicide is selected from the group consisting of titanium silicide, cobalt silicide and nickel silicide.

3. The semiconductor device according to Claim 1, wherein gates of transistors in said DRAM section and logic section are all P-N gates.

4. The semiconductor device according to Claim 1, which has a bit contact connecting the DRAM section with a bit line and a contact plug connecting to the source-drain in the logic section, with each of these contacts being formed of a metal material.

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5. A method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements, wherein silicidation of all the surfaces of the source-drain regions and the gate surfaces that constitute transistors in the DRAM section and the logic section is carried out concurrently in one and the same step.

6. The method of manufacturing a semiconductor device according to Claim 5, wherein said step of silicidation comprises forming a metal film over the entire surface of the substrate, and thereafter performing a heat treatment to remove the unreacted metal film.

7. The method of manufacturing a semiconductor device according to Claim 6, wherein said metal film is selected from the group consisting of titanium, cobalt and nickel.

8. The method of manufacturing a semiconductor device according to Claim 5, wherein dopant implantation into gates are carried out concurrently with formation of the source-drain regions that constitute transistors in the DRAM section and the logic section, and thereby P-N gates are formed.

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9. The method of manufacturing a semiconductor device according to Claim 5, which further comprises the step of forming a bit contact connecting the DRAM section with a bit line and a contact plug connecting to the source-drain in the logic section, with each of these contacts being formed of a metal material.

10. A semiconductor device having a memory cell section and an adjacent circuit section, wherein silicide layers are formed on all the surfaces of the source-drain regions and the gate surfaces of transistors in the memory cell section and the adjacent circuit section.

11. The semiconductor device according to Claim 10, wherein said silicide is selected from the group consisting of titanium silicide, cobalt silicide and nickel silicide.

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12. A method of manufacturing a semiconductor device having a memory cell section and an adjacent circuit section, wherein silicidation of all the surfaces of the source-drain regions and the gate surfaces of transistors in the memory cell section and the adjacent circuit section is carried out concurrently in one and the same step.

13. The method of manufacturing a semiconductor device according to Claim 12, wherein said step of silicidation comprises forming a metal film over the entire surface of the substrate, and thereafter performing a heat treatment to remove the unreacted metal film.

14. The method of manufacturing a semiconductor device according to Claim 13, wherein said metal film is selected from the group consisting of titanium, cobalt and nickel.

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